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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/775,167	02/01/2001	Yasushi Kubota	55561 (820)	7275

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EXAMINER	
NELSON, ALECIA DIANE	

ART UNIT	PAPER NUMBER
2675	

DATE MAILED: 10/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/775,167	KUBOTA ET AL.	
	Examiner	Art Unit	
	Alecia D. Nelson	2675	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1 statement*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. ***Claims 1 and 25*** are rejected under 35 U.S.C. 102(b) as being anticipated by Nakao (U.S. Patent No. 5,289,518).

With reference to **claims 1 and 25**, Nakao teaches a shift register circuit provided with a plurality of register blocks each having a flip flop (31-34) that operates in synchronization with a clock signal (CK1) (see column 3, lines 31-36), and a transfer gate (NAND) for controlling the clock signal supplied to the flip-flop (see column 4, lines 1-7); the plurality of register blocks being serially connected together (see Figure 4), and the transfer gate (NAND, CK1) of a corresponding register block being brought into an ON-state only in a specified period during which an output of the flip-flop of the corresponding register block changes (see Figure 5). With further reference to claim 25, Nakao teaches the use of a control circuit (35) for outputting a control signal to each of the transfer gates (see column 3, lines 39-41).

With reference to **claim 2**, Nakao teaches that when the level of the input signal inputted to each register block and the level of the output signal outputted from the

register block differ from each other, the transfer gate of the register block is brought into an ON-state (see Figure 5)

With reference to **claim 3**, Nakao teaches that the flip-flop is a D-type flip-flop (see Figure 4), and the register block (31-34) has a logic operation section (61-64) for executing a logic operation of an input signal (data signal) of the register block, an output signal (Q) of the register block and controls the transfer gate to be turned on and off based on a signal representing a logic operation result of the logic operation section (see column 3, lines 37-58).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. **Claims 4, 5, and 14** are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakao.

With reference to **claim 4**, Nakao fails to teach the usage of an SR-type flip-flop, however the examiner takes official notice in that it would have been obvious to one having ordinary skill in the art at the time of the invention to allow the usage of an SR-type flip-flop as opposed to the D-type flip-flop, wherein it is well known to use these types of flip-flops interchangeably or in combination with one another.

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention to allow usage of a D or SR-type flip-flop in the device similar to that which is taught by Nakao in order to thereby provide a alternative method for reducing power consumption in the shift register.

With reference to **claims 5 and 14**, Nakao teaches that the register block receives inputs (CK1) to a clock input terminal of the flip-flop of the register block for bringing the output of the flip-flop into a retained state in a period during which the transfer gate is in an OFF-state (see Figure 5).

While not specifically stating that the input is generated by a retainment circuit generating a retainment signal, it can still be seen in the figure that the flip-flop is in a retained state in a period during which the transfer gate is in an OFF-state, therefore the input (CK1) carries out the same function as the claimed retainment signal.

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention to allow the usage of the input as a retainment signal for retaining the output of the flip-flop when the transfer gate is in an OFF-state in order to thereby provide a shifter register with a reduction in power consumption.

5. ***Claims 6, 9-12, 17-19, and 22-24*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakao as applied to **claim 1** above, and further in view of Erhart et al. (U.S. Patent No. 5,572,211).

With reference to **claims 6, 9-11, 19, and 22-24**, while teaching the usage of a shift register as explained above; Nakao fails to specifically teach the details of the display device for which the shift register is used.

With reference to **claims 6 and 19**, Erhart et al. teaches that a shift register is used in a liquid crystal display scanner to generate horizontal sampling pulses comprising a plurality of pixels arranged in a matrix form (20), a plurality of data signal lines for supplying image data to be written into the plurality of pixels, a plurality of scanning signal lines for controlling the image data to be written into the pixels, a data signal line drive circuit for driving the data signal lines and a scanning signal line drive circuit for driving the scanning signal lines (see column 6, lines 17-54; Figures 1-2). With further reference to **claims 9-11 and 22-**24 Erhart et al. fail to specifically teach that the data signal line and the scanning signal line drive circuits are formed on a substrate identical to that of the plurality of pixels, however such an arrangement is well known in the art. As well as a polysilicon thin film transistor and the temperature range for forming the TFT on the glass substrate.

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention to allow the usage of the display device similar to that which is conventional in the art as taught by Maekawa to be used as the display device for the shift register taught by Nakao in order to thereby provide a display device wherein lower power consumption of the shift register can be achieved.

With reference to **claims 12, 13, and 15**, Nakao fails to teach that the shift register circuit includes a level shifter for shifting the level of the clock signal a level not lower than the clock signal input level of the flip-flop; wherein the level shift circuit is brought into an operating state every register block when the flip-flop changes; that when the level of the input signal and the level of the output signal from the register block are different the transfer gate is brought into an ON-state and level shift circuit is brought into an operating state; and OFF-state signal circuit that inputs to the clock input terminal of the level shift circuit an OFF-state signal of a level at which no current flows through the level shift circuit in the period during which the transfer gate is in the OFF-state.

Erhart et at. teaches an integrated circuit for generating output voltages for a series of column driver output circuits used to drive a LCD display (see abstract). The column driver circuit includes a level shift block (166) for shifting the level of the clock signal so that the level of the clock signal becomes not lower than the clock signal input level of the flip-flop; wherein the clock signal is level shifted to provide a level shifted clocking signal which is coupled to the clock input terminals of each of the flip flops of the shift reregister (158) (see column 10, lines 20-30). Further it is taught that when the level of the input signal and the level of the output signal from the register block are different the transfer gate is brought into an ON-state and level shift circuit is brought into an operating state (see column 10, lines 39-62); and OFF-state signal circuit that inputs to the clock input terminal of the level shift circuit an OFF-state signal of a level at which no current flows through the level shift circuit in the period during which the

transfer gate is in the OFF-state (column 10, lines 30-38). With further reference to **claim 16**, teaches that the level shift circuit (166) is connected to a power source line (VDD) and a ground line (VSS), and the register block has a disconnecting circuit for disconnecting either one of the power source line and the ground line of the level shift circuit in the period during which the transfer gate is in the OFF-state (see column 10, line 20-62).

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention to allow the usage of the level shifter as taught by Erhart et al. in a system similar to that which is taught by Nakao to thereby provide an integrated circuit for an LCD wherein the shift register circuit is operated at a lower voltage, thereby allowing power consumption to be further reduced.

With reference to **claims 17 and 18**, Nakao teaches that the flip-flop is a D-type flip-flop (see Figure 4), and the register block (31-34) has a logic operation section (61-64) for executing a logic operation of an input signal (data signal) of the register block, an output signal (Q) of the register block and controls the transfer gate to be turned on and off based on a signal representing a logic operation result of the logic operation section (see column 3, lines 37-58).

Nakao fails to teach the usage of an SR-type flip-flop, however the examiner takes official notice in that it would have been obvious to one having ordinary skill in the art at the time of the invention to allow the usage of an SR-type flip-flop as opposed to

the D-type flip-flop, wherein it is well known to use these types of flip-flops interchangeably or in combination with one another.

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention to allow usage of a D or SR-type flip-flop in the device similar to that which is taught by Nakao in order to thereby provide a alternative method for reducing power consumption in the shift register.

6. **Claims 7 and 20** are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakao in view of Maekawa as applied to **claim 6 and 19** above, and further in view of Kawaguchi et al. (U.S. Patent No. 5,602,561).

With reference to **claims 7 and 20**, Nakao teaches all that is required as explained above however fails to teach that the output pulse width of the data signal line drive circuit is controlled by controlling a pulse width of the input signal.

Kawaguchi et al. teaches that an output pulse width of the data signal line drive circuit is controlled by controlling a pulse width of an input signal (s) inputted to the register block of the first stage of the shift register circuit (see column 4, lines 39-46).

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention to allow the adjusting the output pulse width of the data signal line drive circuit similar to that which is taught by Kawaguchi et al. to be used in a device similar to that which is taught by Nakao in order to thereby provide a display device which will operate more efficiently.

7. **Claims 8 and 21** are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakao in view of Maekawa and Kawaguchi et al. as applied to **claim 7 and 20** above, and further in view of Zenda (U.S. Patent No. 5,111,190).

With reference to **claims 8 and 21**, while teaching all that is required as explained above there fails to be any disclosure of generating a side black region displayed on an upper side and lower side of the display screen by writing black while increasing the pulse width of the input signal.

Zenda teaches a side black region is displayed on an upper side and a lower side of an image display screen (see Figures 1-7) by writing a black signal into all the data signal lines while increasing the pulse width of the input signal inputted to the register block of the first stage of the shift register circuit so that all the data signal lines are brought into an active state by the data signal line drive circuit (see column 4, lines 44-59).

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention to allow the display of non-display data by increasing the pulse width, similar to that which is taught by Zenda, in a device similar to that which is taught by Nakao, Maekawa, and Kawaguchi et al. in order to thereby provide a display device which provides non-display regions wherein the display device consumes less power.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alecia D. Nelson whose telephone number is 571-272-7771. The examiner can normally be reached on Monday-Friday 9:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on 571-272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

9. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

adn/ADN
September 19, 2005

SUMATI LEFKOWITZ
SUPERVISORY PATENT EXAMINER